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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,210	09/24/2004	Wolfdietrich Georg Kasperkovitz	ItoMo40912	7415
23662	7590	11/21/2006	EXAMINER	
ROBERT M. MCDERMOTT, ESQ. 1824 FEDERAL FARM ROAD MONTROSS, VA 22520			NGUYEN, LEON VIET Q	
			ART UNIT	PAPER NUMBER
			2635	

DATE MAILED: 11/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/509,210

Applicant(s)

KASPERKOVITZ, WOLFDIETRICH
GEORG

Examiner

Leon-Viet Q. Nguyen

Art Unit

2635

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 15-20 is/are rejected.
- 7) ☒ Claim(s) 8-14 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

VULE
SUPERVISORY PATENT EXAMINER

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 9-24-04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 9/24/2004 was filed after the mailing date of 9/24/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
- (e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
- (f) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (g) BRIEF SUMMARY OF THE INVENTION.
- (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (i) DETAILED DESCRIPTION OF THE INVENTION.
- (j) CLAIM OR CLAIMS (commencing on a separate sheet).
- (k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a

nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-2, 4-5, 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Kasperkovitz (WO 01/58029A1).

Re claim 1, Kasperkovitz discloses a mirror suppression circuit (fig. 1, fig. 2 a-c, pg. 3 lines 1-11) comprising:
a first quadrature signal path (i.e. the output of 10 to 4) coupled between quadrature signal input and output terminals (fig. 1, pg. 2 lines 1-4) and including
an error correction circuit (10) for correction of amplitude and phase errors in a carrier modulated quadrature signal comprising a pair of in-phase and phase quadrature signal components (pg. 3 lines 26-29), wherein
a quadrature output of the error correction circuit (i.e. the output of 10) is coupled through a first filter circuit (4) for a selection of the quadrature signal to a first quadrature input of an error detection circuit (pg. 3 lines 26-29, fig. 1, 11),

the first quadrature signal path (i.e. the output of 10) is coupled prior to the first filter circuit through a second quadrature signal path (i.e. the output of 10 to 11) to a second quadrature input of the error detection circuit(11),

the error detection circuit (11) detects amplitude and phase errors and provides amplitude and phase control signals to amplitude and phase control inputs of the error correction circuit for a negative feed back (i.e. the output of 11 to 10) of the amplitude and phase errors to the error correction circuit (pg. 3 lines 26-29),

the amplitude control signal varies with at least one of products $I_w * I_{ref}$ and $Q_w * Q_{ref}$ (pg. 4 lines 15-21), and

the phase control signal varies with at least one of products $I_w * Q_{ref}$ and $Q_w * I_{ref}$ (pg. 4 lines 15-21),

I_w and Q_w representing the in-phase and phase quadrature signal components of the quadrature signal at the first quadrature input of the error detection circuit(pg. 3 lines 23-33, pg. 4 lines 10-14), and I_{ref} and Q_{ref} representing the in-phase and phase quadrature signal components of a quadrature reference signal occurring at the negative carrier frequency of the quadrature signal at the second quadrature input of the error detection circuit (pg. 4 lines 1-14, it is well known in that art that).

Re claim 2, Kasperkovitz discloses a mirror suppression circuit, wherein the amplitude control signal varies with $I_w * I_{ref} + Q_w * Q_{ref}$ (pg. 4 lines 15-21), and the phase control signal varies with $I_w * Q_{ref} - Q_w * I_{ref}$ (pg. 4 lines 15-21).

Re claim 4, Kasperkovitz discloses a mirror suppression circuit, wherein the second quadrature signal path is coupled to the first quadrature signal path subsequent to the error correction circuit (fig. 1, the two outputs from the correction circuit 10)

Re claim 5, Kasperkovitz discloses a mirror suppression circuit, wherein the second quadrature signal path includes a second filter circuit for a selection of the quadrature reference signal(22).

Re claim 19, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 4.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3, 6, 15-18 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasperkovitz (WO 01/58029A1) in view of Komarek (US6408008).

Re claim 3, Kasperkovitz fails to teach a mirror suppression circuit, wherein the second quadrature signal path includes an inverter that provides signal inversion in obtaining the quadrature reference signal. However, Komarek teaches inverting an audio input signal with respect to an audio output signal (col. 49 lines 56-59).

Therefore taking the combined teachings of Kasperkovitz and Komarek as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the inverter of Komarek into the mirror suppression circuit of Kasperkovitz to provide echo cancellation or echo balance of signals (col. 49 lines 60-62).

Re claim 6, Kasperkovitz teaches a mirror suppression circuit, wherein the second filter circuit being substantially identical to the first filter circuit (fig. 1, components 9 and 22). Kasperkovitz fails to teach wherein the second quadrature signal path includes the inverter coupled between the first quadrature signal path and the second filter circuit. However it would have obvious to one of ordinary skill in the art to couple the inverter of Komarek between the first quadrature signal path and the second filter circuit to provide echo cancellation prior to filtering (col. 49 lines 60-62).

Re claim 15, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 3.

Re claim 16 and 20, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 4.

Re claim 17, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 5.

Re claim 18, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 6.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasperkovitz (WO 01/58029A1) in view of Leyonhjelm (WO 99/23756).

Re claim 4, Kasperkovitz fails to teach a mirror suppression circuit, wherein the second quadrature signal path is coupled to the first quadrature signal path subsequent to the error correction circuit. However Leyonhjelm teaches using four inputs, two of which are from the input and two from the output, that are coupled together through a phase adjuster (fig. 3A, pg. 17 lines 12-18).

Therefore taking the combined teachings of Kasperkovitz and Leyonhjelm as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the feedback technique of Leyonhjelm into the mirror suppression circuit of Kasperkovitz so that no off-line calibration is needed in the system (pg. 17 lines 14-15).

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasperkovitz (WO 01/58029A1) in view of Walton et al (US7054378) and further in view of Leyonhjelm (WO 99/23756).

Re claim 7, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claims 1. Furthermore, Kasperkovitz teaches an RF input stage for converting a received radio frequency into center frequency quadrature signals by means of an oscillator signal (pg. 2 lines 22-24). Kasperkovitz further teaches a polyphase center frequency filter coupled to the RF input stage to filter the center frequency signals (pg. 3 lines 1-4). However Kasperkovitz fails to teach an IF stage for a selective amplification of the IF signal. Kasperkovitz also fails to teach the quadrature input of the mirror suppression circuit coupled to a quadrature output of the mixer stage. Walton teaches a demodulator that filters and amplifies a received signal and then downconverts that signal to an intermediate frequency (col. 15 lines 50-53, 154). Leyonhjelm teaches using four inputs, two of which are from the input and two from the output, that are coupled together through a phase adjuster (fig. 3A, pg. 17 lines 12-18).

Therefore taking the combined teachings of Kasperkovitz, Walton, and Leyonhjelm as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the demodulator of Walton and the feedback technique of Leyonhjelm into the mirror suppression circuit of Kasperkovitz to provide samples and further demodulate those samples to generate a stream of modulation symbols to be sent to a data processor (Walton col. 15 lines 53-56), which further cancels interference (Walton fig. 5) and also to use the feedback loop so that no off-line calibration is needed in the system (Leyonhjelm pg. 17 lines 14-15).

Allowable Subject Matter

9. Claims 8-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The allowable subject matter in claim 8, used in combination with claim 7, pertains to the use of the second filter selecting the quadrature reference signal occurring at the negative carrier frequency of the quadrature IF signal. The allowable subject matter in claims 11 and 13, used in combination with claim 7, pertain to a first and second multiplier.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2635

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/


VU LE
SUPERVISORY PATENT EXAMINER